

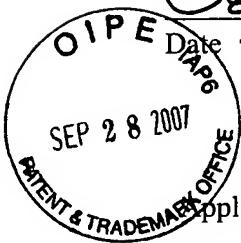
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PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

*September 25, 2007* *Alexandra Beggs Jr*

Alexandra Beggs



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Paul A. LaBerge Attorney Docket No.: 501128.01  
Patent No. : US 6,898,648 B2 Serial No. : 10/081,652  
Issue Date : May 24, 2005 Filed : February 21, 2002  
Title : MEMORY BUS POLARITY INDICATOR SYSTEM AND METHOD FOR  
REDUCING THE EFFECTS OF SIMULTANEOUS SWITCHING OUTPUTS (SSO)  
ON MEMORY BUS TIMING

REQUEST FOR CERTIFICATE OF CORRECTION

*Certificate*  
*OCT 02 2007*  
*of Correction*

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Item (54)	"MEMORY BUS POLARITY INDICATOR SYSTEM AND METHOD FOR REDUCING THE AFFECTS OF SIMULTANEOUS SWITCHING OUTPUTS	--MEMORY BUS POLARITY INDICATOR SYSTEM AND METHOD FOR REDUCING THE EFFECTS OF SIMULTANEOUS SWITCHING OUTPUTS (SSO) ON MEMORY BUS TIMING--

*OCT 2 2007*

(SSO) ON MEMORY BUS  
TIMING”

Item (57), Line 7	“data contained each”	--data contained in each--
Column 1, Line 3	“THE AFFECTS OF”	--THE EFFECTS OF--
Column 1, Line 16	“system are clock””	--system are--
Column 2, Line 8	“in response rising”	--in response to rising--
Column 2, Line 36	“modem synchronous”	--modern synchronous--
Column 3, Lines 11-12	“thereby undesirable shifts”	--thereby undesirably shifts--
Column 4, Line 39	“of bits the data words”	--of bits of the data words--
Column 4, Line 51	“contained each read data”	--contained in each read data--
Column 7, Line 14	“data bus DATA bus”	--data bus DATA--
Column 8, Line 54	“that in the memory”	--that the memory--
Column 8, Line 62	“would typically includes”	--would typically include--
Column 9, Line 16	“for the inverted next”	--or the inverted next--
Column 9, Line 26	“is coupled to tell with”	--is coupled with--
Column 9, Line 32	“either the NDW<1:N> for”	--either the NDW<1:N> or--
Column 9, Line 67	“determines number of bits”	--determines the number of bits--
Column 10, Line 12-13	“determines number of bits”	--determines the number of bits--
Column 11, Line 6	“inverted DL-DM words”	--inverted D1-DM words--
Column 11, Line 52	“data bus inversion word”	--data bus inversion words--
Column 11, Line 56	“an segment”	--a segment--
Column 11, Line 66	“inversion bit I1 bit is cleared”	--inversion bit I1 is cleared--
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Column 12, Line 38	“there are 8 data word”	--there are 8 data words--
Column 12, Line 46	“in the DBI<1:*> may need”	--in the DBI<1:8> word may

		need--
Column 13, Line 47	“such as output”	--such output--
Column 14, Line 23	“word, and”	--word; and--
Column 14, Lines 29-30	“on an associated data masking pins.”	--on an associated data masking pin.--
Column 14, Line 37	“plurality of data masking pin”	--plurality of data masking pins--
Column 15, Line 44	“and apply an active a data”	--and apply an active data--
Column 16, Line 10	“to a clocks signal; and”	--to a clock signal; and--
Column 16, Line 40	“received write data words invert or not invert”	--received write data words to invert or not invert--
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The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

OCT 2 2007

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: Sept. 24, 2007

By:



Edward W. Bulchis, Reg. No. 26,847  
Customer No. 27,076  
Dorsey & Whitney LLP  
1420 Fifth Avenue, Suite 3400  
Seattle, WA 98101  
(206) 903-8785  
Attorney for Applicant(s)

EWB:tdp

Enclosures:

Postcard

Form PTO-1050 (+ copy)

501128.01 req cert correct

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : US 6,898,648 B2  
DATED : May 24, 2005  
INVENTOR(S) : Paul A. LaBerge

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invert"

invert--

MAILING ADDRESS OF SENDER:

**DORSEY & WHITNEY LLP**  
**1420 Fifth Avenue, Suite 3400**  
**Seattle, Washington 98101**

Patent No. US 6,898,648 B2

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FORM PTO-1050 (REV. 3-82)

501128.01 PTO 1050

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Attorney for Applicant(s)

EWB:tdp

Enclosures:

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501128.01 req cert correct

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MAILING ADDRESS OF SENDER:

Patent No. US 6,898,648 B2

**DORSEY & WHITNEY LLP**  
**1420 Fifth Avenue, Suite 3400**  
**Seattle, Washington 98101**

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**FORM PTO-1050 (REV. 3-82)**

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